In the Specification:

Please replace paragraph **[0012]** with the following paragraph:

-- **[0012]** Referring to Fig. 2c, the filling layer 24 is etched. The etching of the sidewalls of the spacers 20 is restricted because of a high etching selectivity of the undoped polysilicon or the amorphous silicon with the SiN of the spacers 20. Therefore, if an anisotropic etching method with good selectivity is performed, the undoped polysilicon or the amorphous silicon, which fills the gaps between the spacers 20, remains without being removed by the etching process. The etching solution used to etch the undoped polysilicon or the amorphous silicon is preferably ~~HNO3+CH3COOH+HF~~ HNO_3+CH_3COOH+HF.--.

Please replace paragraph **[0016]** with the following paragraph:

-- **[0016]** From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed method ~~prevent~~ prevents changes of cell characteristics due to voids by obviating the formation of voids in gaps between gate spacers in the deposition of BPSG. In particular, the illustrated method of fabricating a flash memory cell comprises: forming spacers to isolate and protect a gate area; depositing undoped polysilicon; etching the polysilicon by an anisotropic etching; and depositing BPSG.--.